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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/856,999 | 05/30/2001 | Klaus Steinigke | P01,0162 | 7847 |

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FOLEY & LARDNER
777 EAST WISCONSIN AVENUE
SUITE 3800
MILWAUKEE, WI 53202-5308

| EXAMINER | |
|---|---|
| SHAH, CHIRAG G | |
| **ART UNIT** | **PAPER NUMBER** |
| 2664 | |

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/856,999 | STEINIGKE, KLAUS | |
| | Examiner | Art Unit | |
| | Chirag G Shah | 2664 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/30/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/30/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (U.S. Patent No. 5,805,571) in view of Zwan et al. (U.S. Patent No. 5,448,574), hereinafter Zwan.

Referring to claim 6, Yamaguchi discloses in figure 1 and in column 3, lines 29 to column 4, lines 20 of a method for confirming the serviceability and correct use of switching units in a switching device (units 11, 21, and 31) using connecting cables (multicore cables such as C11 and C21) which connect plug connections to one another, the switching units comprising fault monitoring devices (a comparator circuit 212 for comparing bit by bit the string of digital signal samples with the core probe signal supplied via the monitoring core 111 and a probe signal inserting circuit 217 sends outputs of the comparator circuit 212, the core probe signal from circuit 216 for detecting any faulty connection of the whole cable C21) which respond to specific faults in transmission signals, the method comprising the steps of:

emitting test signals to an end of relevant ones of said connecting cables [as disclosed in figure 1 and in column 3, lines 29-60, unit 11 provided with a core probe signal generating circuit 112 and a probe signal inserting circuit 113 supplies core probe

signal to the monitoring core 111 at a prescribed timing. 113 also inserts a cable probe signal for detecting the connected state of the cable C11 on a whole cable basis]

evaluating output signals occurring at each of the other ends of the relevant ones of said connecting cables [as disclosed in figure 1 and in col. 3, lines 62 to column 4, lines 65, a comparator circuit 212 compares bit by bit the string of digital signal samples with the core probe signal supplied via the monitoring core 111 and a probe signal inserting circuit 217 sends outputs of the comparator circuit 212, the core probe signal from circuit 216 for detecting any faulty connection of the whole cable. If the plurality of signals transferred over cable C11 are normal, the output comparator remains "0', if any discrepancy arises , the circuit 212 will give an output of "1"].

Yamaguchi discloses in the abstract, figure 1 and in column 4, lines 41 to column 5, lines 18 that upon evaluating the output signals, generates a faulty connection indicating signal in response to any discrepancy between them and supplies the output to the display unit. Yamaguchi, however fails to disclose transmitting said test signals via the relevant ones of said connecting cables when said fault monitoring devices detect specific faults in said transmission signals. Zwan discloses in column 14, lines 15-30 of generating a first protocol signal and supplying the first protocol signal to a communication device, receiving a second protocol signal form the communications device containing the first protocol signal embedded therein, extracting the embedded first protocol signal form the second protocol signal, and comparing the embedded first protocol signal to the original first protocol signal to determined communications device performance. Zwan further discloses in figures 9A, lines 10-27 of the processor 22 collecting data from test modules and reporting results such as errors and alarms on display 35.

Zwan further discloses in figures 1 and 2 along with figure 10B and respective portions of the specification that the display 35 is a part of the common control device 20, which receives the collected, evaluated and analyzed data from the processor. Thus, establishing that when fault monitoring devices processor detects a specific fault in the transmission signal (which may be DS1, DS3, SONET, ATM as disclosed in the abstract), the processor reports test signals via relevant connecting cables to the display 35 of the controller. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Yamaguchi to include the transmitting of test signals via the relevant ones of connection cable as a loopback to the controller as taught by Zwan in order to facilitate controller with reports of faults/errors to ensure efficient maintenance and enhancement of the fault conditions.

Referring to claim 7, Yamaguchi discloses in column 6, lines 17-36 wherein corrupted synchronization signals are used as transmission signals having faults [if any one of the cores of the cable C11 is broken, the time slot corresponding to the broken signal lacks a signal, the output of the comparator will indicate abnormality and indicate a faulty connection establishing that corrupted synchronization signals as transmission signals having faults] as claim.

Referring to claim 8, Yamaguchi fails to disclose that corrupted signals of ATM transmission may be used as transmission signals having faults. Zwan discloses in the abstract, figure 1, figure 3 and respective portions of the specification wherein corrupted synchronization signals of ATM transmission may be used along with DS1, DS3, SONET as transmission signals having faults as claim. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Yamaguchi to include the Zwan's teachings in order to facilitate

controller with reports of faults/errors of corrupted synchronization signals of ATM transmission to ensure efficient maintenance and enhancement of the fault conditions.

Referring to claim 9, Yamaguchi discloses in figure 1 of a circuit for confirming the serviceability and correct use of switching units in a switching device (units 11, 21 and 31), said switching device (communications apparatus) including switching units connected to one another by plug-in connecting cables (cables such as C11, C12), the circuit comprising:

> a fault signaling device (217 and 317) located in each switching unit (11, 21, 31), said fault signaling device capable of emitting fault reporting signals when specific faulty transmission signals occur [As disclosed in column 3, lines 62 to column 4, lines 62, the outputs of comparator circuits and the other outputs of the branching circuits are supplied to the display unit 41 via an indicating signal generating circuit. Furthermore, as disclosed in column 4, lines 62 to column 5, lines 18, faulty connection on any of the cables C11 through C14, C21, C22 is indicated on the display unit 41 immediately upon occurrence. ]; and

Yamaguchi discloses in figure 1 and in column 3, lines 62 to column 4, lines 20 of unit 11 capable of emitting transmission signals as test signals. Yamaguchi fails to disclose of a test device connected to said switching units, said test device capable of emitting transmission signals as test signals corrupted by faults to one set of switching units, whereby said test device checks other switching units via the connecting cables for occurrence of fault reporting signals. Zwan discloses in column 14, lines 15-30 of generating a first protocol signal and supplying the first protocol signal to a communication device, receiving a second protocol signal form the communications device containing the first protocol signal embedded therein, extracting the

embedded first protocol signal form the second protocol signal, and comparing the embedded first protocol signal to the original first protocol signal to determined communications device performance. Zwan further discloses in figure 1 of a test device including several modules including a common control module 20, a SONET module 40, and an ATM processor module 90. Zwan further discloses in figures 9A-B and 10A-B and respective portions of the specification of simultaneous testing of DS-1 cable, DS-3 cable and OC-12 optical cable. In the test in one example, a desired DS3 stream is fed into SONET module through switch 200. SONET module maps DS3 signal into an OC-12 signal which passes to customer mux 280. The mux performs its internal demapping to extract the DS3 signal, which is routed to DS3 line interface and then routed back to DS3 processor for evaluation and analysis. Such tests are simultaneously performed to determine the functionality under true working conditions. Furthermore, the processor collects data from all three active test modules and reports results such as errors and alarms on display 35. Thus, establishing that Test Device sends transmission signals to switching units and simultaneous testing enable the test device to check other switching units for occurrence of fault reporting signals. Therefore, it would have been obvious to one of ordinary skills in the art to modify the teachings of Yamaguchi to include performing simultaneous testing of other switching units as taught by Zwan in order to facilitate controller with reports of faults/errors to ensure efficient maintenance and enhancement of the fault conditions existing in all switching units.

Referring to claim 10, Yamaguchi discloses in figure 1 wherein said test device [11] is connected to said switching units (211 and 212) via separate connecting lines as claim.

*Conclusion*

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**Or faxed to:**

(703)305-3988, (for formal communications intended for entry)

**Or:**

(703)305-3988 (for informal or draft communications, please label "Proposed" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
October 28, 2004

Ajit Patel
Primary Examiner